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Abstract
In this thesis, a frequency synthesizer for RF front-end applications is presented. The sigma-delta modulator (SDM) technique is adopted to reduce the phase noise within the synthesizer bandwidth and decrease fractional spur.

The design concern of frequency synthesizer will focus on improving phase noise performance and to decrease the circuit non-linearity. Moreover, the inverse Chebyshev function is used to synthesize the noise transfer function (NTF) of the SDM. The digital SDM with the OSR of 20 and the bandwidth of 0.475MHz has been verified by cell-based flow, and the other circuits of the frequency synthesizer have been implemented based on the TSMC 0.18μm 1.8V 1P6M CMOS process. The mathematic simulator, MATLAB, is employed to co-simulate the tracking behavior of the entire fraction-N frequency synthesizer which has tuning range from 5.1968GHz to 5.2107GHz and 0.0396MHz resolution.
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